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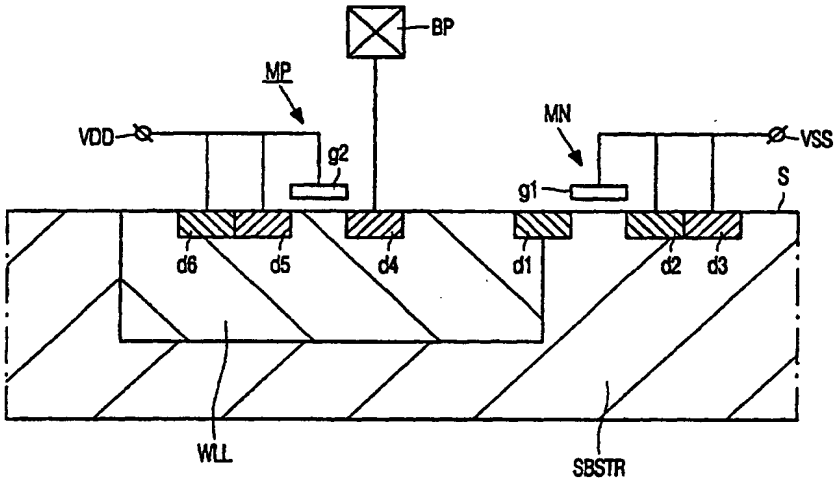
(54) Title: AN INTEGRATED CIRCUIT PROVIDED WITH ESD PROTECTION MEANS



(57) Abstract

An integrated circuit provided with ESD protection means comprising a silicon–controlled rectifier whose n–well (WLL), if the substrate (SBSTR) of the integrated circuit is of the p–type, is connected to the VDD supply instead of to the bonding–pad (BP) to which electronic circuitry is connected. Consequently, the anode is only formed by the p^+ diffusion (d4) in the n–well (WLL). Therefore, negative voltages are allowed at the bonding pad (BP) because the junction is not forward–biased. Thus, an ESD protection towards the VSS is obtained. Additionally, a PMOST (MP) is used as an ESD protection towards the VDD.

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An integrated circuit provided with ESD protection means.

The invention relates to an integrated circuit comprising protection means for protecting against electrostatic discharge, which protection means is provided on a substrate of a first conductivity type, and said protection means comprises a first highly doped surface area of a second, opposite, conductivity type, a second highly doped surface area of the second conductivity type, a first gate insulated from the surface of the integrated circuit, which first gate is positioned so as to form a first MOS-device in conjunction with the first and the second highly doped surface areas, and a third highly doped surface area of the first conductivity type, which is located directly beside the second highly doped surface area, the first gate and the second and the third highly doped surface areas are electrically coupled to a first reference terminal, the substrate being provided with a well of the second conductivity type, the well being partly stretched out into the region of the first highly doped surface area, and the well being provided with a fourth highly doped surface area of the first conductivity type which is electrically coupled to a bonding pad BP of the integrated circuit.

Such an integrated circuit is known from the general state of the art. The fourth highly doped surface area, the well, the substrate, and the second highly doped surface area together form an SCR element (Silicon-Controlled Rectifier). The SCR element is in fact a four-layer pnpn (or npnp) structure with connections on the outer p-layer and the outer n-layer. One of the connections is formed by the fourth highly doped surface area and the other one of the connections is formed by the second highly doped surface area. A purpose of the protection means is to avoid damage in the integrated circuit caused by electrostatic discharge (ESD). In general, diodes, Field oxide NMOS, thin oxide NMOS, and Silicon Controlled Rectifiers are used as ESD protection means.

A problem of the known ESD protection means is that if for instance the bonding pad is negatively biased with respect to the first reference terminal, no n^+ diffusion is to be electrically connected to the bonding pad in a p-substrate CMOS integrated circuit, because the n^+ diffusion at the bonding-pad would be forward biased with respect to the substrate. This would cause a current through the substrate, which adversely affects the behaviour of the integrated circuit. For the same reason, an n^+/p diode and an NMOS as ESD protection means coupled to the first reference terminal is not allowed.

It is an object of the invention to solve the above-mentioned problem.

An inventive integrated circuit of the type described in the opening paragraph is therefore characterized in that the well further comprises a fifth highly doped surface area of the first conductivity type, a second gate insulated from the surface of the integrated circuit, and a sixth highly doped surface area of the second conductivity type which is located directly beside the fifth highly doped surface area, and in that the second gate is positioned so as to form a second MOS-device in conjunction with the fourth and the fifth highly doped surface areas, and in that the second gate and the fifth and the sixth highly doped surface areas are electrically coupled to a second reference terminal. As a result, the protection means provide for two protection paths. Let us for example assume that the first conductivity type is the p-type and the second conductivity type is the n-type. Then one of the two protection paths, hereinafter referred to as first protection path, comprises a p^+n diode, which is formed by the p^+ diffusion (the fourth highly doped surface area) at the bonding pad and the n-well (i.e. the well if the second conductivity type is the n-type). Thus, the first protection path forms an ESD-protection between the bonding pad and the second reference terminal. The other one of the two protection paths, hereinafter referred to as the second protection path, is formed by the SCR of which, in this example, the outer p-layer is formed by the fourth p^+ doped surface area in the n-well, and of which the outer n-layer is formed by the second n^+ doped surface area in the p-type substrate. In this example, in which the first conductivity type is the p-type and the second conductivity type is the n-type, the protection means according to the invention do not have an n^+ diffusion which is electrically connected to the bonding-pad. This is in contrast with the known protection means.

The invention will be described in more detail with reference to the accompanying drawings, in which:

Figure 1 is a cross-sectional view of a part of an integrated circuit having input protection means for protecting against electrostatic discharge; and

Figure 2 shows a simplified electrical circuit diagram corresponding to the part of the integrated circuit shown in Figure 1.

In these Figures, parts or elements having like functions or purposes bear the same reference symbols.

Figure 1 is a cross-sectional view of a part of an integrated circuit having input protection means for protecting against electrostatic discharge. It is assumed by way of example that the integrated circuit comprises a p-type substrate SBSTR. As a result the well WLL is of the n-type, and will hereinafter be referred to as the n-well WLL. The integrated circuit is provided with highly doped surface areas d1, d2 and d6 of the n-type, which will hereinafter be referred to as n^+ areas, and with highly doped surface areas d3, d4 and d5 of the p-type which will hereinafter be referred to as p^+ areas. A first gate g1 and the n^+ areas d1 and d2 jointly form a first MOS-device MN. The first gate g1, the n^+ area d2, and the p^+ area d3 are electrically connected to a first reference terminal VSS. A second gate g2 and the p^+ areas d4 and d5 jointly form a second MOS-device MP. The second gate g2, the p^+ area d5, and the n^+ area d6 are electrically connected to a second reference terminal VDD. The p^+ area d4, the p^+ area d5, and the n^+ area d6 are located within the n-well WLL. The n^+ area d1 is only partially located within the n-well WLL. The p^+ area d4 is electrically connected to a bonding pad BP of the integrated circuit. The bonding pad BP is for instance an input pad which is electrically connected to an input of an electronic circuit (not shown in the Figures) of the integrated circuit. Very often, a gate of a MOS-transistor of the electronic circuit is electrically connected to the input pad. Such a MOS-transistor can very easily be damaged by an electrostatic discharge on its gate because the gate of such a MOS-transistor has a very high input impedance. The protection means, as shown in figure 1, limits the voltage at the bonding pad, caused by an electrostatic discharge, for both positive and negative voltage spikes. An important difference between the protection means of Figure 1 and known protection means is that, irrespective of the polarity of the voltage spikes there will be no current flowing through the substrate SBSTR. This can be attributed to the fact that, using the protection means of Figure 1, no n^+ area is connected to the bonding pad BP since the n-well WLL is connected, via the n^+ area d6, to the second reference terminal VDD, whereas in known protection means the n-well WLL is connected to the bonding-pad BP, causing substrate currents, which adversely affects the behaviour of the electronic circuit on the integrated circuit.

Figure 2 shows a simplified electrical circuit diagram corresponding to the part of the integrated circuit shown in Figure 1. The source and the back gate of the second MOS-transistor MP, which are formed respectively by the p^+ area d5 and the n-well WLL, are connected to the second reference terminal VDD. The second gate g2 is also connected to the second reference terminal VDD. A drain of the MOS-transistor MP, being the p^+ area d4, is connected to the bonding pad BP. A first bipolar transistor T_1 is with an emitter connected to the bonding pad BP, with a collector to a base of a second bipolar transistor T_2, and with a

base to a collector of the second bipolar transistor T_2. The collector of the first bipolar transistor T_1 is connected via a first resistor R_1 to the first reference terminal VSS. The collector of the second bipolar transistor T_2 is connected via a second resistor R_2 to the second reference terminal VDD. The emitter of the second bipolar transistor T_2 is connected to the first reference terminal VSS. The first resistor R_1 is caused by the resistance of the substrate SBSTR between the n^+ area d1 and the p^+ area d3. The second resistor R_2 is caused by the resistance of the n-well WLL between the n^+ area d1 and the n^+ area d6. The first and second bipolar transistors T_1 - T_2, and the first and second resistors R_1 - R_2 together form the SCR the operation of which is well known.

It will be evident that the invention is not restricted to the examples described above, but that within the framework of the invention a great many variations are possible to the expert. In the examples described above, the conductivity types may be reversed, in which case, of course, the voltages to be applied must be adapted.

CLAIM:

1. An integrated circuit comprising protecting means for protection against electrostatic discharge, which protection means is provided on a substrate (SBSTR) of a first conductivity type, and said protection means comprises a first highly doped surface area (d1) of a second, opposite, conductivity type, a second highly doped surface area (d2) of the second conductivity type, a first gate (g1) insulated from the surface (S) of the integrated circuit, which first gate (g1) is positioned so as to form a first MOS-device (MN) in conjunction with the first (d1) and the second (d2) highly doped surface areas, and a third highly doped surface area (d3) of the first conductivity type which is located directly beside the second highly doped surface area (d2), the first gate (g1) and the second (d2) and the third (d3) highly doped surface areas are electrically coupled to a first reference terminal (VSS), the substrate (SBSTR) being provided with a well (WLL) of the second conductivity type, the well (WLL) being partly stretched out into the region of the first highly doped surface area (d1), and the well (WLL) being provided with a fourth highly doped surface area (d4) of the first conductivity type which is electrically coupled to a bonding pad (BP) of the integrated circuit, characterized in that the well (WLL) further comprises a fifth highly doped surface area (d5) of the first conductivity type, a second gate (g2) insulated from the surface (S) of the integrated circuit, and a sixth highly doped surface area (d6) of the second conductivity type, which is located directly beside the fifth highly doped surface area (d5), and in that the second gate (g2) is positioned so as to form a second MOS-device (MP) in conjunction with the fourth (d4) and the fifth (d5) highly doped surface areas, and in that the second gate (g2) and the fifth (d5) and the sixth (d6) highly doped surface areas are electrically coupled to a second reference terminal (VDD).

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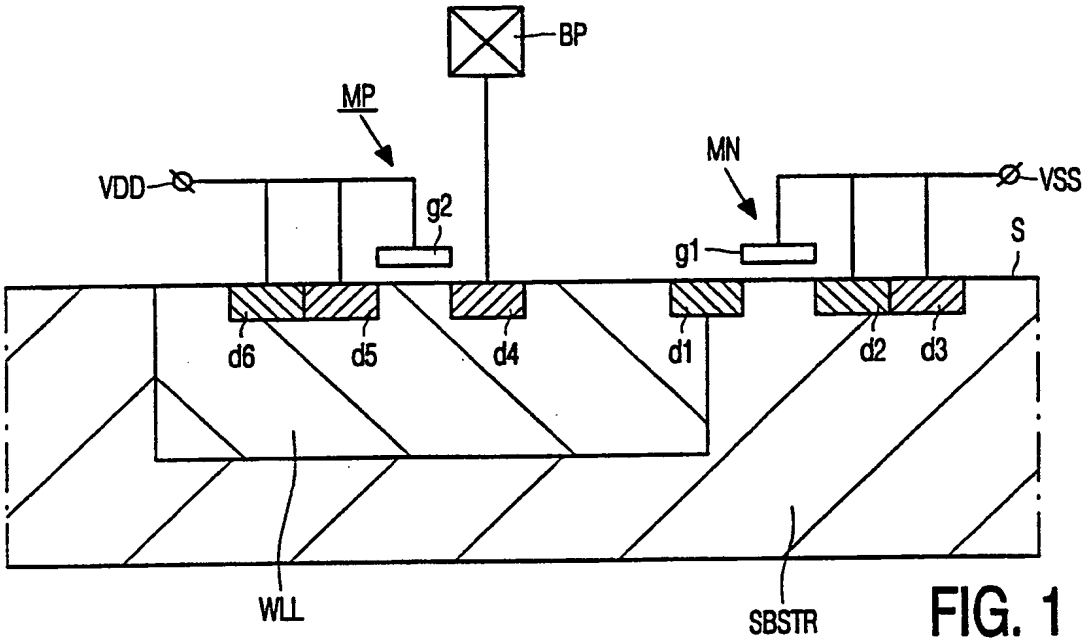
BP
MP
MN
VDD
VSS
g2
g1
S
d6
d5
d4
d1
d2
d3
WLL
SBSTR

FIG. 1

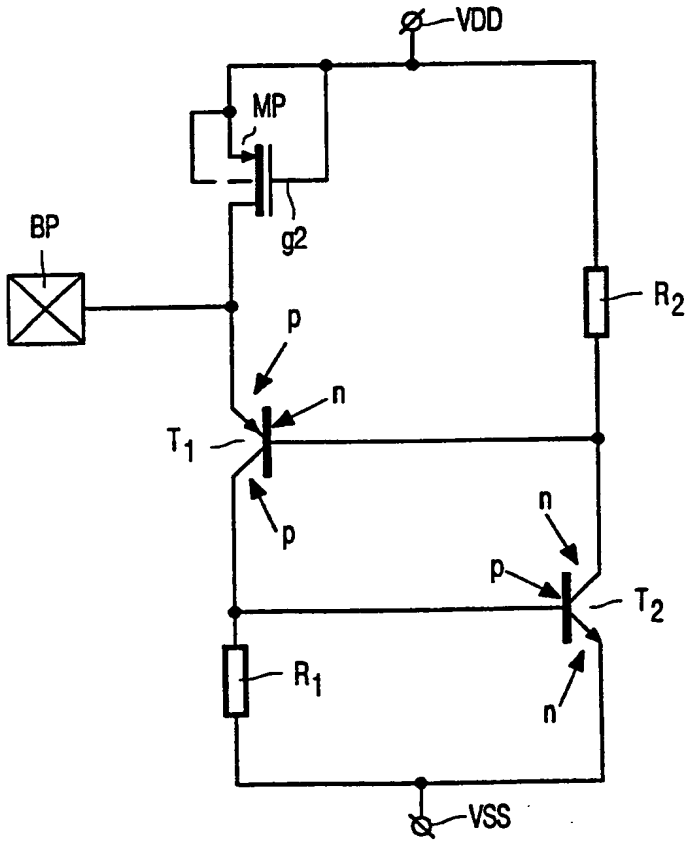
VDD
MP
g2
BP
R2
p
n
T1
p
n
p
T2
R1
n
VSS

FIG. 2

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP 99/05517

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L27/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 615 073 A (NATIONAL SEMICONDUCTOR CORP) 25 March 1997 (1997-03-25) the whole document ---	1
Y	EP 0 774 785 A (AT&T CORP) 21 May 1997 (1997-05-21) column 5, line 20 - line 30; figure 2 ---	1
A	EP 0 782 192 A (SAMSUNG ELECTRONICS CO LTD) 2 July 1997 (1997-07-02) abstract; figures ---	1
A	WO 94 03928 A (HARRIS CORP) 17 February 1994 (1994-02-17) abstract; figures 7,8B ---	1

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A	US 5 455 436 A (INDUSTRIAL TECHNOLOGY RESEARCH INSTITUTE) 3 October 1995 (1995-10-03) abstract; figures	1

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EP 774785 A	21-05-1997	US 5744840 A	28-04-1998
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US 5455436 A	03-10-1995	NONE	

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